Errata to Publications from Martin Kumm

Unfortunately, it happens that mistakes appear, even after several rounds of serious proof-readings by myself, my co-authors, colleagues and finally the reviewers. Any error is really unfortunate and really annoys me. But I think the best way to deal with it is to publish the corrections. This document collects and corrects the errors I made in my previous publications (as far as I know them). If you find errors, don't hesitate to tell me, please!

An FPGA-Based Linear All-Digital Phase-Locked Loop [1]

There is a sign error in the sub-filter defined in equation (29), correct would be:

$$Z_{-90}(z) = 1+jz^{-1}$$

Thanks to Carl Leuschen for this hint!

Pipelined Adder Graph Optimization for High Speed Multiple Constant Multiplication [2]

In the comparison with Levent Aksoy's HCUB-DC+ILP method [3], filter instance A30 required an implementation cost (icost) of 52958 instead of 2958. This leads to an average icost of 117536 instead of 109203 and reduced the relative area reduction from 15.5% as given in the text to 9%. The corrected table can be found in [4]. Thanks to Levent Aksoy for the hint to this unfortunate typo.

Multiple Constant Multiplication with Ternary Adders [5]

The sign bit $s_{v/w} \in \{-1, 1\}$ in (1) should be correctly $s_{v/w} \in \{0, 1\}$.

An Efficient Softcore Multiplier Architecture for Xilinx FPGAs [6]

The sentence "The remaining four FFs can be used to delay the a_n inputs without cost in this case." is wrong. The remaining four FFs in the slice are not accessible anymore as the `AX`/`BX`/`CX`/`DX` inputs of the slice are already in use. Thanks to Ken Chapman for pointing out this mistake. However, by using the LUT configuration of the softcore multiplier of George Walters III [7] (which was presented at the time when [6] was submitted) the FFs become accessible.

Multiple Constant Multiplication Optimizations for Field Programmable Gate Arrays [4]

The coefficient order of the transposed FIR filter shown in Fig. 1.2(b) is reversed to the definition in (1.1). Fig. 1 shows the corrected FIR structures.

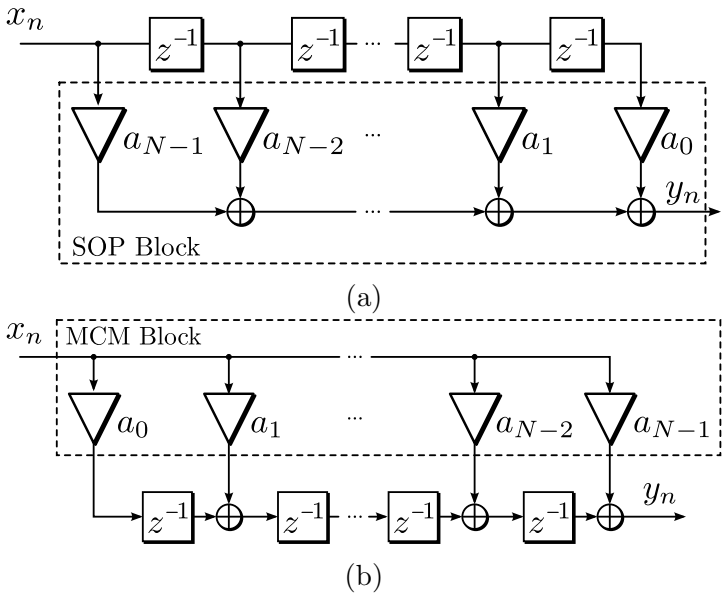

Figure 1: Structure of an FIR filter in (a) direct form and (b) transposed form

Another error happened in constrain C2 of PMCM ILP Formulation 3 (page 97): The index in the ILP variable has to be w' and not w, so the correct constraint is:

$$\text{C2:} \quad \left.\begin{aligned} x^s_{(u,v,w)} - \sum_{(u',v',w')\in\mathcal{T}^s \,|\, w'=u} x^{s-1}_{(u',v',w')} \leq 0 \\ x^s_{(u,v,w)} - \sum_{(u',v',w')\in\mathcal{T}^s \,|\, w'=v} x^{s-1}_{(u',v',w')} \leq 0 \end{aligned}\right\} \begin{array}{l}\text{for all } (u,v,w)\in\mathcal{T}^s \\ \text{with } s = 2\ldots S\end{array}$$

Optimization of Constant Matrix Multiplication with Low Power and High Throughput [8]

The sentence

"Stage X_0 contains the N different unit vectors of length N which correspond to the inputs."

has to be replaced by

"Stage X_0 contains the M different unit vectors of length N which correspond to the inputs."

Optimal Constant Multiplication using Integer Linear Programming [9]

In constraint C4b, the index of the sum should go to $S_{\max}$ and not $S_{\max} - 1$. Correct is the following:

$$\text{C4b:} \qquad \sum_{s=S_{\min}}^{S_{\max}} \varphi_{a,i,s} = 1 \qquad \forall a = 1 \ldots N_{\mathrm{A}}, i \in \{\ell, \mathrm{r}\} \ .$$

In constraint C6b, the sum index and the index for the different constraints were reversed. Correct is the following:

$$\text{C6b:} \qquad \sum_{a=0}^{N_{\mathrm{A}}} o_{a,j} = 1 \qquad \forall j = 1 \ldots N_{\mathrm{O}}$$

Pipelined Compressor Tree Optimization Using Integer Linear Programming [10]

There is an index error in the ILP formulation. $M_{e,c+c'}$ and $K_{e,c+c'}$ has to be replaced by $M_{e,c'}$ and $K_{e,c'}$, respectively, and $k_{s-1,e,c+c'}$ has to be replaced by $k_{s-1,e,c-c'}$. This affects C1 and C2 and the correct constraints are:

$$\text{C1:} \quad N_{s-1,c} \leq \sum_{e=0}^{E-1} \sum_{c'=0}^{C_e-1} M_{e,c'}\, k_{s-1,e,c-c'} + ID_s \qquad \text{for } s = 1 \ldots S-1,\ c = 0 \ldots C-1$$

$$\text{C2:} \quad N_{s,c} = \sum_{e=0}^{E-1} \sum_{c'=0}^{C_e-1} K_{e,c'}\, k_{s-1,e,c-c'} \qquad \text{for } s = 1 \ldots S-1,\ c = 0 \ldots C-1$$

Advanced Compressor Tree Synthesis for FPGAs [11]

The same index error as in [10] appeared here for C1 and C2, as well as for the C1', which has to be:

$$\text{C1':} \quad N_{s-1,c} \leq \sum_{e=0}^{E-1} \sum_{c'=0}^{C_e-1} M_{e,c'}\, k_{s-1,e,c-c'} \qquad \text{for } s = 1 \ldots S-2,\ c = 0 \ldots C-1$$

Karatsuba with Rectangular Multipliers for FPGAs [12]

In the alternative form for Karatsuba as given in (4) has a sign error. The equation

$$a_1 b_0 + a_0 b_1 = (a_1 - a_0)(b_1 - b_0) + M1 + M4$$

with $M1 = a_0 b_0$ and $M4 = a_1 b_1$ has to be replaced by

$$a_1 b_0 + a_0 b_1 = (a_0 - a_1)(b_1 - b_0) + M1 + M4 \tag{1}$$

to be correct. The generic from given as (12) is correct and does not contain this error.

References

[1] M. Kumm, H. Klingbeil, and P. Zipf, "An FPGA-Based Linear All-Digital Phase-Locked Loop," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, no. 9, pp. 2487–2497, 2010.

[2] M. Kumm, P. Zipf, M. Faust, and C.-H. Chang, "Pipelined Adder Graph Optimization for High Speed Multiple Constant Multiplication," in *IEEE International Symposium on Circuits and Systems (ISCAS)*, 2012, pp. 49–52.

[3] L. Aksoy, E. Costa, P. Flores, and J. Monteiro, "Optimization of Gate-Level Area in High Throughput Multiple Constant Multiplications," in *European Conference on Circuit Theory and Design (ECCTD)*, 2011, pp. 609–612.

[4] M. Kumm, "Multiple Constant Multiplication Optimizations for Field Programmable Gate Arrays," Ph.D. dissertation, Springer Wiesbaden, Wiesbaden, Oct. 2015.

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[7] E. G. Walters, "Partial-Product Generation and Addition for Multiplication in FPGAs with 6-Input LUTs," *Asilomar Conference on Signals, Systems and Computers*, pp. 1247–1251, 2014.

[8] M. Kumm, M. Hardieck, and P. Zipf, "Optimization of Constant Matrix Multiplication with Low Power and High Throughput," *IEEE Transactions on Computers*, vol. 66, no. 12, pp. 2072–2080, 2017.

[9] M. Kumm, "Optimal Constant Multiplication using Integer Linear Programming," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 65, no. 5, pp. 567–571, 2018.

[10] M. Kumm and P. Zipf, "Pipelined Compressor Tree Optimization Using Integer Linear Programming," in *IEEE International Conference on Field Programmable Logic and Application (FPL)*. IEEE, 2014, pp. 1–8.

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[12] M. Kumm, O. Gustafsson, F. de Dinechin, J. Kappauf, and P. Zipf, "Karatsuba with Rectangular Multipliers for FPGAs," in *IEEE Symposium on Computer Arithmetic (ARITH)*, 2018.